Temperature Compensated Low Voltage MOSFET Radiation Sensor: Proof of Concept and A Case Study

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***Abstract*— This paper presents a proof of concept performed on a new and very simple CMOS circuit configuration that implements a radiation dosimeter based on the threshold voltage difference (VTH) principle. The circuit used does not use resistors and all the transistors work in strong inversion, their mobility factor being completely canceled by the proposed architecture. Its operation exploits the relationship between radiation and VTH shifting, which allows, through a circuit configuration, to compensate for temperature variation and amplify the reaction to radiation, making it ideal for integrated industrial applications due to its simplicity and good operation. The circuit was designed for operation in areas naturally at risk of radiation, for example nuclear power plants or radiological clinics. Its advantage over other circuits that perform similar functions is mainly its low cost and simplicity of design.**

Keywords—CMOS dosimeters, radiation dosimetry, temperature compensation.

I. INTRODUCTION

Radiation detection and measurement currently has many different applications, such as medicine, industry, the environment, national security, non-proliferation of weapons or national defense [1], [2], [3]. Currently there are different types of sensors on the market [4], [5], [6], and most of them are based on CMOS (Complementary Metal-Oxide-Semiconductor) technology in silicon (Si) [4], [6], [7], [8]. The latter have qualities that are impossible to match with traditional circuits such as thermoluminescent (TLD) or diode-based [9], [10], [11].

There are basically two types of radiation: particle (typically neutrons or protons) and photons (X or Gamma radiation) [12], [13]. The latter is the one received when a cancer treatment or diagnosis is made. In these cases, it is common practice to measure the Total Ionizing Dose (TID) in Gray (Gy) [14], which is defined as the absorption of one Joule of radiation energy per kilogram of matter.

In a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) integrated circuit, electron-hole pairs are generated in the oxides and insulators due to ionizing radiation [13]. This effect could lead to the degradation and failure of the device [15], but it is also feasible to use it to determine the radiation dose through the TID measurement. In these circuits, some short-term single-event effects, called Single Event Effects, or SEEs, occur, which are present for a short time interval, causing momentary changes in device properties. However, there are other effects that can become permanent [16], [17]. The latter, called long-term effects, constitute the operating principle of this proposal.

When radiation is detected using silicon circuits, the change in threshold voltage (VTH) with the radiated dose has been commonly used as a measurement parameter. One of the main problems when using MOS circuits for dosimetry is the displacement of VTH due to temperature, an effect that can lead to incorrect readings [8]. While this is not a serious problem for high dose measurements, special care must be taken to avoid this effect when measuring low radiation doses. In the literature there are different ways to approach the problem of thermal compensation, either with elaborate circuits or configurations [5], [6], [10] or at the cost of external processing [14]. All of these approaches involve the over-allocation of circuit resources, and their respective impact on integration costs.

This work presents a simple and novel differential configuration to measure the radiation TID, which takes advantage of the difference between the threshold voltages of the NMOS and PMOS transistors (N and P channel MOSFETs respectively) for their operation [18], which which constitutes, as far as the authors are aware, an original and unpublished proposal. This arrangement allows the implementation of a radiation sensor with cancellation of thermal effects and power supply variation with rejection values comparable to that of a voltage reference generator, by using only 8 transistors and without the need for external processing, thus allowing its complete integration. The proposed circuit does not use resistors, and is suitable for low-cost standard CMOS technologies, as no additional manufacturing steps are required.

The rest of the document is organized as follows: Section II provides a brief explanation of the physical principle on which the operation of the sensor is based. Then, in Section III, the proposed circuit is presented. Section IV explains the methodology used in the design and the simulation results are reported. In Section V the reader will find an analysis of the immunity of the sensor with the variation of the manufacturing

process, and finally the conclusions are synthesized in Section VI.

II. Physical Principle

A high energy photonic impact can generate thousands of electron-hole pairs in the oxide in the structure of an MOS integrated circuit, which represents the main reason for almost all TID effects. The charge accumulation mechanism described in [13] is illustrated in Fig. 1. This figure represents the energy band diagram for a MOSFET with substrate p, channel n and positive gate polarization. When the electron-hole pair is created, the electron will move toward the gate and the hole will move toward the oxide-Si interface due to polarization. In this process, the generated gaps that do not recombine will move towards the oxide-Si interface and are trapped there. At threshold, trapped charges are predominantly positive for p-channel MOSFETs and negative for n-channel MOSFETs.

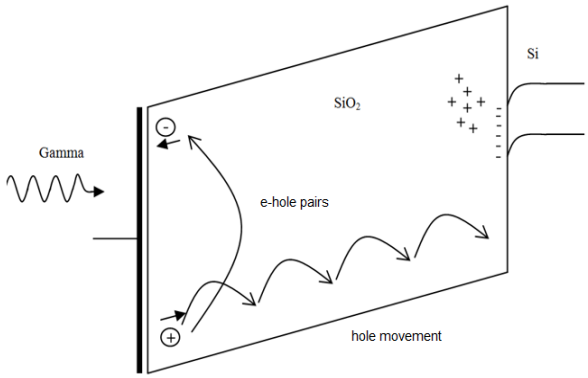

Fig. 1. Band diagram of a MOS device after receiving ionizing radiation, according to [13].

The charges trapped in the oxide, called NOX, change the threshold voltage of the CMOS device as follows:

$$\Delta V_{TH} = -\frac{q.t_{ox}^2.N_{ox}}{\varepsilon_{ox}}\ [V] \qquad (1)$$

In (1), q is the charge of the electron, tox is the thickness of the oxide and εox is the permittivity of the oxide. The threshold voltage differential (ΔVTH) is negative. This means that the displacement produces a decrease in VTH for the NMOS transistor and an increase in the absolute value of VTH for PMOS devices. This effect, represented in the graph in Fig. 2, is the physical principle on which the present proposal is based.

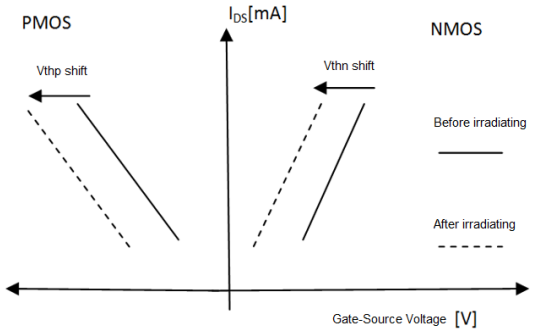

Fig. 2. Shift of the threshold voltage due to the charges trapped in the oxide, according to [10].

III. Proposed Configuration

For the implementation of a device that is capable of performing an indirect measurement of the TID, the circuit of Fig. 3 is proposed. In this scheme, a displacement of Vref shows the shifting of the threshold voltage VTH upon exposure of the device to a source of ionizing radiation.

The architecture is based on the threshold voltage difference principle without added parasitic transistors [18], [19], [20].

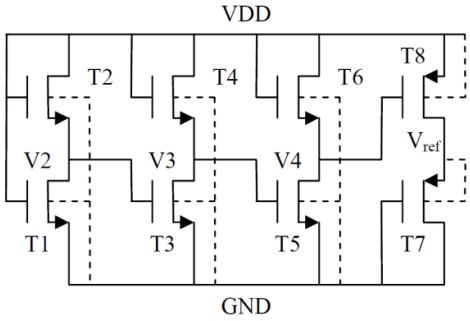

Fig. 3. Proposed configuration for the dosimeter.

The operation of the circuit of Fig. 3 is explained from the analysis of two independent groups of transistors NMOS (T1 to T6) and PMOS (T7 and T8), as explained in detail in [18]. Each branch or group of transistors fulfills different functions, and therefore their designs must be approached independently. Transistors T2 to T4 work saturated while T1 works in linear zone. Together, T1 through T4 work to stabilize the V3 voltage with respect to VDD variations [21]. Transistors T5 and T6 are in saturation and convert voltage V3 (referenced to GND) to voltage VDD-V4, referenced to VDD. Finally, transistors T7 and T8 will act together as a VTHN and VTHP differentiator (subtractor), generating an output voltage Vref that depends on both VTHs.

It is observed that there are no added resistances, which makes the circuit ideal for integration. This also frees the proposed intrinsic dependence of resistances on temperature [22], [23]. It should be noted that each branch of the circuit of Fig. 3 is formed by a pair of transistors of the same type, which makes it possible to cancel mobility in each one of them. In this way, it is possible to demonstrate that the output voltage Vref will depend only on the difference in threshold voltages, as observed in (2).

$$V_{ref} = \frac{\frac{\sqrt{\beta_2}}{\delta} V_{THN} - (1-\sqrt{\beta_4})\, V_{THP}}{\sqrt{\beta_4}}\ [V] \qquad (2)$$

where β_2 y β_4 are defined as:

$$\beta_2 = \frac{(\frac{W}{L})_3}{(\frac{W}{L})_4} \qquad (3)$$

$$\beta_4 = \frac{(\frac{W}{L})_7}{(\frac{W}{L})_8} \qquad (4)$$

In (2), δ is the Memelink parameter [24], which typically varies between 1 and 1.5. In this case, a δ = 1.15 was used for

the simulations based on previous manufacturing experiences with the same technology [21].

The equations found are based on mathematical models that coincide with SPICE level 1 (level = 1). This is common practice in the design of electronic circuits since it allows a relatively simple conceptual analysis and does not present a problem as long as the simulations carried out with more complex and precise models corroborate, within the expected margin of error, the predictions reached.

As previously stated, the proposed circuit minimizes the effects of temperature variation, while allowing measurement of incident TID radiation. This is feasible since the absolute value of VTH for both types of N and P transistors decreases with temperature, while, when considering the variation with radiation, the absolute value of VTHN decreases while VTHP increases (see Fig. 2). When deriving (2) with respect to temperature, we find the temperature coefficient of the output voltage Vref. The result is shown in (5):

$$\frac{\partial V_{REF}}{\partial T} = \frac{-\frac{\sqrt{\beta_2}}{\delta}\propto_{VTHN}+(1-\sqrt{\beta_4})\propto_{VTHP}}{\sqrt{\beta_4}} \left[\frac{V}{^\circ C}\right] \quad (5)$$

where αV_{THN} y αV_{THP} are the temperature coefficients for the threshold voltages of a NMOS and PMOS transistor respectively. To get $(\partial V\_REF)/\partial T=0$, the ratio of temperature coefficients must be equal to:

$$\frac{\propto_{VTHP}}{\propto_{VTHN}} = \frac{\frac{\sqrt{\beta_2}}{\delta}}{(1-\sqrt{\beta_4})} \quad (6)$$

If (5) and (6) are met simultaneously, (2) will display the output voltage with temperature compensation. As previously stated, the displacement of threshold voltages due to radiation is induced in the same direction. This means that, for radiation, there is no cancellation; on the contrary, the effect is additive. In this way, we will have an output that shows dependence on radiation, but independent of temperature and VDD variations.

TABLE I
TRANSISTORS SIZING (AMI 1.5µM)

Transistor	*W/L* [µm/µm]
T1	12/54.8
T2	54.8/12
T3	24.5/12
T4	12/24.5
T5	16.3/12
T6	12/16.3
T7	12/40
T8	40/12

IV. DESIGN EXAMPLE AND SIMULATIONS

A priority issue is to visualize in which VDD voltage range the design equations shown above are valid. It should be clear to the reader that the polarization conditions of the transistors will change with the supply voltage, causing the devices to be correctly polarized only in a certain range. To detect this operating zone, a DC analysis is proposed, the result of which is shown in Fig. 4. This figure shows the DC sweep for the temperature (T) that varies between 27 ° C and 127 ° C in steps of 10 ° C.

The circuit shown in Fig. 3 was designed using the BSIM3 model for 1.5 AMm AMI technology. This model is chosen in particular in order to be able to contrast results with those obtained in [18] and [21]. It is worth noting that the directions of the VTH shifts on which the present proposal is based are independent of the integration technology used but depend on the type of incident radiation.

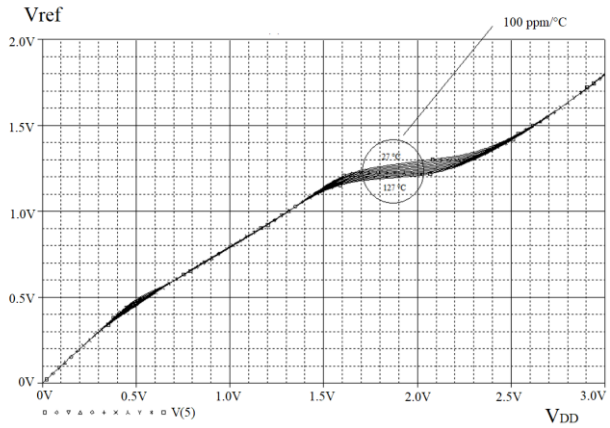

Fig. 4. Vref as a function of V_{DD} for different temperatures.

The dimensions of the transistors used for the simulation are indicated in Table I. Long channel devices were chosen to minimize the effect of channel length modulation. From this basic concept, the design was made following equations (2) to (6) with the addition of the restrictions given in [18].

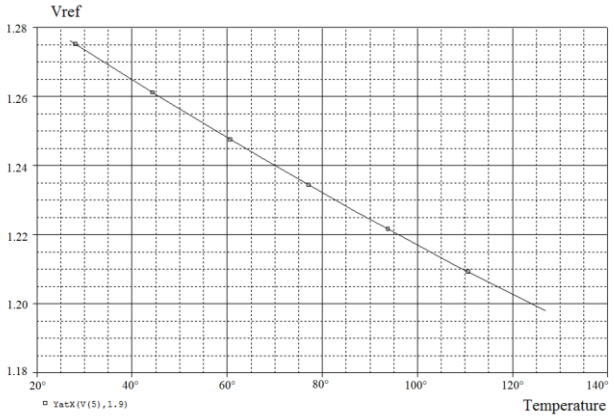

Fig. 5. Output voltage vs. temperature for V_{DD}= 1.9V

To study the independence of the circuit with respect to temperature, simulations were made varying the temperature between 27 and 127 ° C.

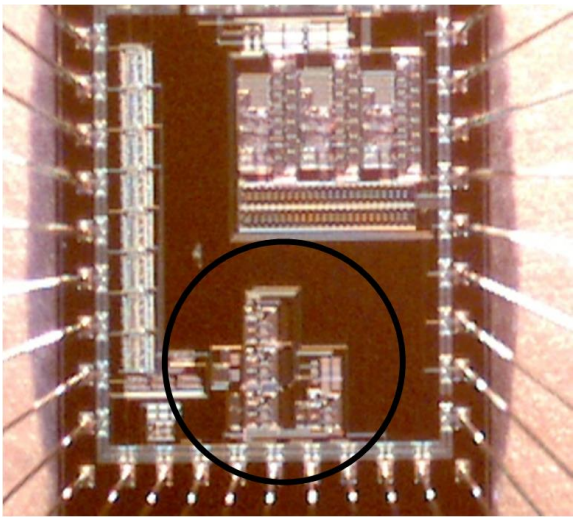

Fig. 6. A microphotograph of a multipurpose chip. The referred cell is marked with a circle

Fig. 5 shows the results obtained for a VDD = 1.9V, without radiation effect. From this figure it is possible to determine a shift of only 80mV for the entire temperature range proposed. From these simulations and with the help of Fig. 4, a Temperature Coefficient of 100 ppm / ºC is verified for the Vref output, stable throughout the simulated range of temperatures and voltages.

A core circuit containing the idea was fabricated in AMI 1.5um, proving the idea is feasible and providing some important measuring data [21]. A microphotograph of the Integrated Circuit is shown in figure 6. In future works, it is planned to re-use this fabricated core for further testing under different conditions.

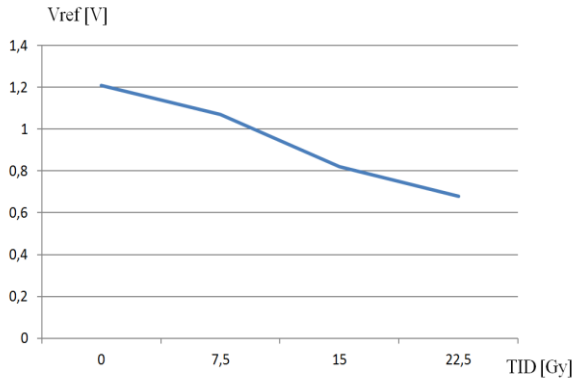

Fig. 7. Output voltage vs. Radiation dose

Changes in VTH with radiation were simulated assuming the variations reported in [25]. Fig. 7 shows the results obtained for a range of 0 to 25 Gy of gamma radiation, at room Temperature of 300K. It can be seen that the circuit has a monotonically decreasing and practically linear response for the wide range of TID chosen. The good sensitivity to the average radiation obtained stands out, which is located at a value of 21.5 mV / Gy. If this value is compared with other MOS dosimeter works analyzed, this circuit presents a higher average sensitivity than that observed in [10] and [14], which report values of 10mV / Gy and 6.44mV / Gy respectively. Because of scaling reasons, temperature changes of Vref are not significant enough for including them in Fig. 7. They are shown instead in figure 9.

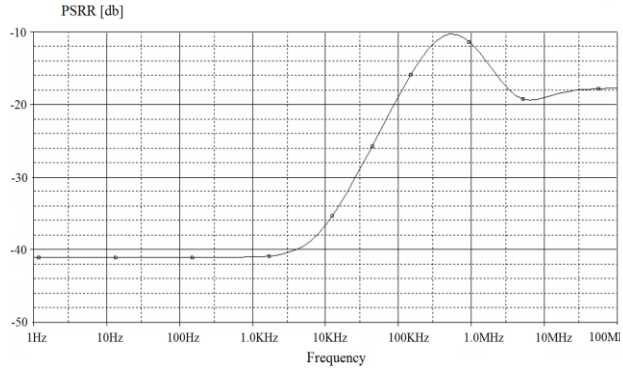

Fig. 8. PSRR from proposed circuit for V_{DD} = 1.9V

The characteristics of sensitivity, linearity and thermal stability presented by the proposed circuit configuration ensure the feasibility of the TID measurement, making it suitable for use as a radiation sensor in a wide range of applications.

Since the circuit also has immunity characteristics to VDD variations, a simulation was performed to determine the Power Supply Rejection Ratio (PSRR), yielding the result shown in Fig. 8. This factor presents a rejection of more than 40 dB for frequencies up to 1kHz, which is the application range of the circuit. This feature becomes important if the circuit is powered by a ripple source.

V. IMMUNITY AGAINST PROCESS VARIATIONS

In CMOS technologies, it is usual to observe variations of the process parameters in high percentages, sometimes higher than 30%. These changes severely impact different parameters of the VLSI (Very Large Scale Integration) circuits [26], [27], such as implanted ion dose, channel length, and threshold voltage, which may vary significantly during fabrication process. This fact will change the behavior of transistors as well. What manufacturers do is identify lots within different corners. These corners then mean that the wafers are grouped according to these process parameters, which traditionally are: Typical NMOS - Typical PMOS (TT); Fast NMOS - Fast PMOS (FF); Fast NMOS - Slow PMOS (FS); Slow PMOS - Fast NMOS (SF) and Slow NMOS - Slow PMOS (SS). In this way, statistical models are increasingly being used when designing Integrated Circuits (ICs) in large scale.

With the corner models given for the 1.5µm technology, an exhaustive evaluation of the circuit of Fig. 3 has been carried out in order to determine the maximum operating limits. The simulation results, where the output voltage Vref is shown as a function of temperature for the different process corners, are synthesized graphically in Fig. 9.

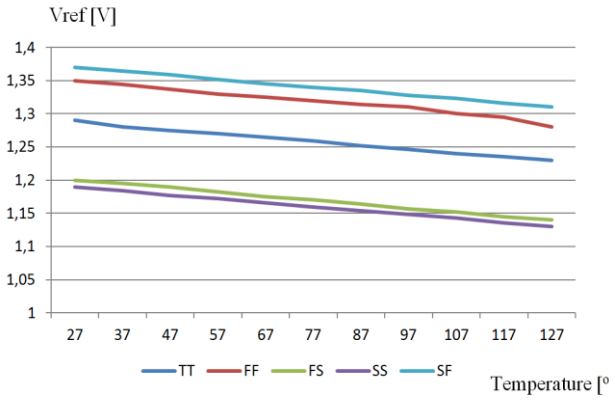

Fig. 9. Output voltage V_{ref} vs. temperature for different process corners

A more detailed report of these results is provided in Table II. From the data obtained, it appears that the Vref output has a standard deviation of less than 10% (7% in this case) between the two extremes (SS and SF) for all simulated temperatures. These results ensure proper operation, without greater dispersion for either case.

TABLE II
SIMULATED VALUES OF V_{REF} [V] FOR DIFFERENT PROCESS CORNERS

Corner *T[°C]*	TT	FF	FS	SS	SF	Desv. Std
27	1,29	1,35	1,2	1,19	1,37	6,79%
37	1,28	1,344	1,195	1,184	1,364	6,76%
47	1,275	1,337	1,19	1,177	1,359	6,77%
57	1,27	1,33	1,182	1,172	1,352	6,75%
67	1,265	1,325	1,175	1,166	1,345	6,77%
77	1,259	1,32	1,17	1,159	1,34	6,81%
87	1,252	1,314	1,164	1,154	1,335	6,82%
97	1,246	1,31	1,157	1,148	1,328	6,84%
107	1,24	1,3	1,152	1,143	1,323	6,75%
117	1,235	1,295	1,145	1,136	1,316	6,79%
127	1,23	1,28	1,14	1,13	1,31	6,63%

VI. CONCLUSIONS

A very simple and yet effective circuit configuration has been presented, based on a CMOS reference voltage scheme for use in dosimetry applications. The proposed circuit does not use resistors, and is suitable for low-cost standard CMOS technologies, since no additional manufacturing steps are needed. Transistors work in strong inversion, for which precise models are available, which simplifies the design procedure, especially in digital CMOS technologies. Mobility compensation is not necessary. Since NMOS transistors do not combine in the same branch with PMOS transistors, the mobility factor is completely canceled. Compensation of the temperature coefficient and VDD variations is performed and a single output voltage proportional to the TID is provided, using a simple relationship between the geometry of the transistors.

It has been verified by simulation that the circuit has an average radiation sensitivity of 21.5 mV / Gy (more than double that of other similar works reported on the subject) and good thermal stability (100 ppm / ºC) and of supply voltage (-40dB of PSRR), in addition to its low voltage operation, thus validating the original proposal.

It has also been verified that the process differences introduce variations of the order of 7%, which is a factor that makes the configuration relatively immune to technological dispersion. The use of the technology proposed in the article is justified in the fact of being able to contrast the results with those obtained in previous works, leaving for future research its adaptation to new integration technologies.

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