

Embedded Radiation Sensor with OBIST Structure for Applications in Mixed Signal Systems

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Abstract— Oscillation-based test (OBT) is a simple and cost-effective VLSI test method for a great number of circuits. In this paper, OBT is applied for the first time for testing a radiation sensor to be used as an embedded VLSI cell in order to implement an OBIST (Oscillation Built-In Self-Test) structure for embedded applications. It is shown that OBT can be implemented with a minimally intrusive switched feedback loop to establish the oscillation. Fault simulation indicates 100% detection of faults in the circuit under test, proving feasibility of the proposed methodology and idea.

Keywords— *fault simulation, mixed signal testing, OBIST, oscillation-based test, VLSI testing.*

I. INTRODUCTION

The great applicability of embedded systems in any field, as well as the added value they provide, makes the development of these systems a strategic area preferred by many companies. Nowadays, embedded systems are found in almost all electronic devices. They have several common characteristics that distinguish such systems from other computing or electronics systems: must satisfy constrained size, energy consumption, reliability, and cost requirements. To meet these restrictions, the design of these kind of systems must take into consideration efficient methods of self-detection malfunctioning to increase their reliability, especially in critical applications—such medical ones—where an error may have catastrophic consequences. In this sense, sensors for medical applications, while mostly analog, are almost always integrated with some digital section.

If mixed signal systems are considered, testing of embedded analog section is a significant challenge. The lack of controllability and observability of its internal nodes is the primary difficulty [1]. Each analog cell has an extremely low number of pins (in some cases none) and doing in these cases the direct test application and evaluating its response is commonly not possible. Another major difficulty that arises when testing analog circuits are absence of standard or widely accepted analog fault models, dependence of analog signals with process variation (performance-sensitive), analog faults do not cause a simple state change in the logic values, not unique signal flow direction, among others. These

reasons usually make specification-based testing very difficult, if not impracticable. Although not standards as their digital counterparts, design-for-test (DFT) methodologies can help overcome many of these drawbacks, implementing functional testing instead of specification-based testing. One proven good technique for some types of analog circuits is the so-called oscillation-based test (OBT) [2-8].

As should be noticed, OBT is a technique that may become very useful when used for implementing the OBIST (Oscillation-Based Built-In-Self-Test). The main idea is to turn the Circuit Under Test (CUT) into an oscillator during the test mode, as has been widely studied for many circuits (operational amplifiers, filters, data converters) [2-4]. During the test phase, a positive feedback loop is created to the CUT, achieving the Barkhausen condition and producing self-sustained oscillations. Faulty behavior is then indicated by measurable deviations in the frequency and/or the amplitude of the oscillations (Typically 5%) when compared to the values under fault-free conditions [3]. OBT looks then as an appealing technique that avoids the necessity of test vector generation, requiring relatively simple measurements, and usually not demanding circuit modifications during the testing phase. These features make Oscillation Based Test an interesting approach when high integration is needed.

It is evident that the OBT implementation will depend strongly on the characteristics of the circuit under test. The introduced feedback that is put in the circuit into an oscillation condition must be thought carefully based on many elements, such as the characteristics of the whole structure that will be tested, the possibility/impossibility of partitioning the CUT, the reachable outputs (from the layout point of view), the analog or digital nature of the signal, etc. Thus, the application of this technique to each new class of circuits becomes an exciting task.

In this paper, we explore the ability of OBT to be applied to a complex circuit such a radiation sensor, proposing the resulting system to be used as an embedded cell for different VLSI purposes. We present a scheme that makes use of a non-linear characteristic in the feedback loop, as seen in Fig.

1. The evaluation of the test quality is made by means of fault simulation.

II. METHODS

The methods used in this research and a brief explanation of its operation will be explained at the following below:

A. The Radiation Sensor Cell

Despite the broad use of digital signal processing in contemporary electronics, analogue circuits are still being used widely in mixed-signal ICs. Especially when implementing radiation sensors, analog solution is still the best way to do it [9-10]. The sensor circuit taken as CUT in this work is reported in [11].

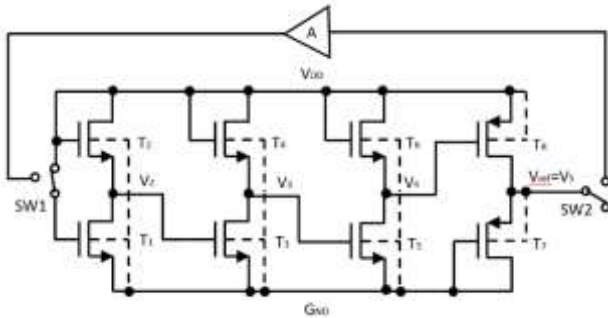


Fig. 1. Block diagram of the proposed cell, including feedback element.

The scheme of the embedded cell is shown in Fig. 1. A quick overview of the sensor cell operation is carried out here for clarity purposes. This explanation can be understood by analyzing two independent chains of transistors, n-type (T1 to T6) and p-type (T7 and T8), as explained in detail in [11]. Each branch accomplishes different uses, and consequently their designs must be taken into account independently. Transistors T2 to T4 work in the saturation region, while T1 works in the linear zone. T1 through T4 serve to stabilize the V3 voltage against VDD deviations. Transistors T5 and T6 work saturated and they transform V3 (with respect to GND) to VDD-V4, with respect to VDD. At the end, transistors T7 and T8 will perform the difference between VTHN and VTHP (subtractor), producing an output voltage V_{ref} that will depend on both VTH.

As it can be noticed, the circuit requires no resistors. This fact makes it especially suited for integration. Readers may also notice that each branch of transistors (see Fig. 1) is implemented with devices of the same type (N or P), making the circuit independent of the mobility, which is cancelled. With these considerations in mind, it is shown that V_{ref} will depend only on the difference in threshold voltages, as can be observed in (1).

$$V_{ref} = \frac{\sqrt{\beta_2} V_{THN} - (1 - \sqrt{\beta_4}) V_{THP}}{\sqrt{\beta_4}} [V] \quad (1)$$

Where β_2 y β_4 are defined as:

$$\beta_2 = \left(\frac{W}{L}\right)_3 \quad (2)$$

$$\beta_4 = \left(\frac{W}{L}\right)_7 \quad (3)$$

In (1), δ is the Meme link parameter [12], which typically varies between 1 and 1.5. In this case, a $\delta = 1.15$ was determined experimentally [13]. The proposed sensor minimizes the effects of temperature variation, while allowing measurement of total ionizing doze (TID) radiation. This can be done due to the fact that absolute value of VTH for both N and P transistors reduce its values with temperature. Simultaneously, considering radiation variations, the absolute value of VTHN decreases while VTHP increases. This was conveniently proved in [11]. The circuit of Fig. 1 was designed and simulated using the BSIM3 model for 1.5 μm AMI technology. The transistors dimension used for the simulation are reported in Table I.

TABLE I. COMPONENT SIZING FOR THE CIRCUIT OF FIG. 1.

Transistor	W/L [$\mu\text{m}/\mu\text{m}$]
T1	12/54.8
T2	54.8/12
T3	24.5/12
T4	12/24.5
T5	16.3/12
T6	12/16.3
T7	12/40
T8	40/12

B. OBT Implementation

Adapting the CUT to become an oscillator requires it to force the oscillation condition. It has been shown [5] that a non-linear feedback loop guarantees sustained oscillations. Consequently, we adopt a positive feedback loop using a non-linear element as [6-7]. The non-linear function presents an abrupt transition between two voltage levels, $+V_{ref}$ and $-V_{ref}$ (See Fig. 2). The benefits of these kind of systems for carrying out the OBT are extensively described by [5-7].

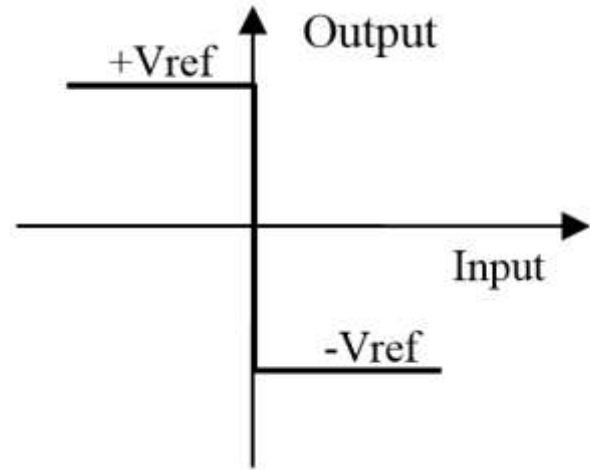


Fig 2. Proposed nonlinear function.

One alternative for implementing the function depicted in Fig. 2 is shown in Fig 3. It is used here as a linear amplifier with high gain followed by a limiter.

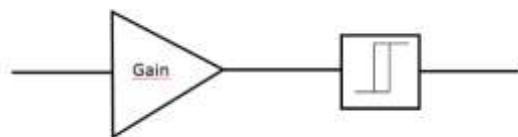


Fig. 3. A possible implementation for the non-linear feedback loop.

The block diagram of the OBT implementation is shown in Fig. 4. As can be observed in this figure, the test strategy manipulates only the input and output of the circuit in order to configure the CUT into the oscillation mode and does not modify its structure. In this way, the test allows a low level of intrusion in the circuit and minimizes the signal degradation in normal mode [8].

During test mode (see Fig. 4), switches SW1 and SW4 isolate the CUT, while SW2 and SW3 connect the feedback path in order to force the oscillation. SW1 and SW4 remain closed in normal mode, while SW2 and SW3 are open.

The depicted function approach is employed for analyzing the system behavior and for finding, in an easy way, the oscillation conditions [8]. Using this concept, the transfer-function of the adopted non-linearity can be expressed as:

$$N(A) = \frac{4 \cdot V_{ref}}{\pi \cdot A} \quad (4)$$

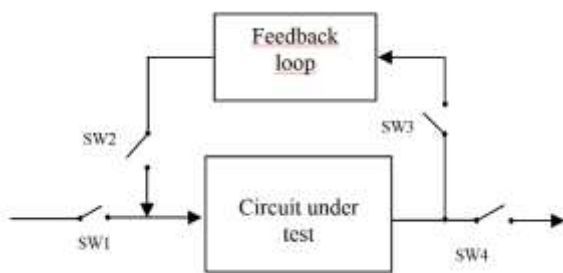


Fig. 4. Block diagram for the oscillator and the feedback block.

Where V_{ref} can be a positive or negative voltage reference level and A is the amplitude of the oscillations.

When analyzing the CUT behavior in test mode, it can be seen that the circuit in Fig. 1 looks similar to a chain of inverters in cascade. Setting the appropriate feedback it will oscillate, at a high frequency, exactly as a ring oscillator made with inverters. Thereby, in order to put the circuit into oscillation, we set a feedback loop (see feedback block A in Fig. 1) to satisfy Barkhausen's condition. When switches SW1 and SW2 are in the position indicated by the above-mentioned figure (switches off), the circuit is in normal mode, working as a dosimeter. When SW1 and SW2 are switched on, the feedback loop is closed and the circuit is placed into an oscillation condition.

The simulated output waveforms for the non-faulty oscillator is presented in Fig. 5. An oscillation frequency f_0 of 33 MHz and amplitude A of 250 mV_{p-p} can be observed.

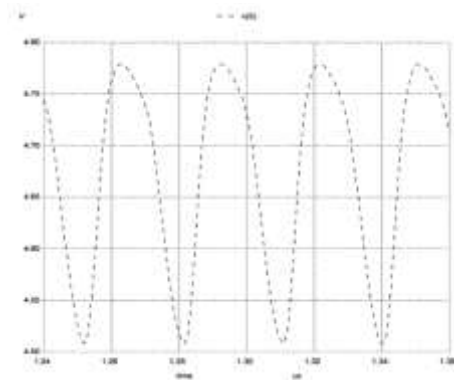


Fig. 5. Oscillator output under non-faulty condition.

As shown in Fig. 4, only the input and output nodes of the circuit are manipulated in order to place the CUT into the oscillation mode. The circuit's core is, therefore, minimally modified to reach the oscillation condition, allowing an extremely low level of intrusion, minimizing the signal degradation in the normal operation mode.

III. RESULTS AND DISCUSSION

This section presents the fault models applied and the report of the simulation results, as well as alternative implementations.

A. Fault Modelling

Conventionally, the efficacy of Oscillation Based Test was assessed at structural level by using single-catastrophic and single-deviation fault-models. By doing this then, it becomes reasonable to use the fault-coverage metric for evaluating the test [2-4]. In the following paragraphs, temperature stability, catastrophic and parametric faults are analyzed at both device and circuit level.

1) Temperature stability

As said before, the sensor circuit presented here for OBIST implementation was analyzed deeply in [11]. Some of the conclusions are presented in this section in order to contribute to the global understanding.

Variations of the manufacturing process are usual in CMOS integration technology and these changes severely impact in some circuits parameters, changing the behavior of transistors. The optimization of VLSI circuits has been traditionally addressed through the use of technology corner models, provided by the manufacturers: Typical NMOS / Typical PMOS (TT); Fast NMOS / Fast PMOS (FF); Fast NMOS / Slow PMOS (FS); Slow PMOS / Fast NMOS (SF); and Slow NMOS / Slow PMOS (SS). In this way, statistical models are increasingly being used when designing Integrated Circuits (ICs).

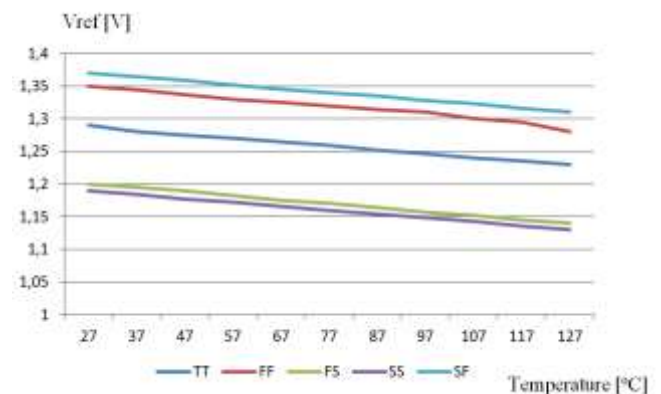


Fig. 6. Output voltage V_{ref} vs. temperature for different process corners.

With the corner models given for the 1.5 μ m technology, an exhaustive evaluation of the circuit of Fig. 1 has been conducted in order to determine the maximum operating limits. The simulation results are synthesized graphically in Fig. 6, where the output voltage V_{ref} is shown as a function of temperature for the different process corners.

A more detailed report of these results is provided in Table II. From the data obtained, it appears that the V_{ref} output has a standard deviation of less than 7% between the two extremes corners (SS and SF) for all simulated

temperatures. These outcomes guarantee correct functioning, without great scattering.

2) *Catastrophic fault injection campaign*

Catastrophic fault simulations were performed in SPICE considering only single fault injection. Open and short circuit faults were modeled by a 10 MΩ and 10 Ω resistor respectively. It is assumed that a fault is detected when the circuit does not oscillate or either the oscillation frequency f0 or amplitude A are out of a tolerance band, defined as ±5% of the free-fault oscillator frequency. The latter means that, if a given CUT presents a frequency and/or amplitude deviation of less than 5% from the nominal values (no fault injected), the circuit is passed as fault-free. This margin has previously shown to account adequately for process variation [8, 11, 14-16] without passing faulty circuits.

As expected, all catastrophic faults (opens and shorts) produce the lack of oscillation in all technology corners. This is because the oscillator circuit leaves all faults in the signal path.

TABLE II. SIMULATED VALUES OF VREF [V] FOR DIFFERENT PROCESS CORNERS

Corner T[C]	TT	FF	FS	SS	SF	Dev. Std
27	1,29	1,35	1,2	1,19	1,37	6,79%
37	1,28	1,344	1,195	1,184	1,364	6,76%
47	1,275	1,337	1,19	1,177	1,359	6,77%
57	1,27	1,33	1,182	1,172	1,352	6,75%
67	1,265	1,325	1,175	1,166	1,345	6,77%
77	1,259	1,32	1,17	1,159	1,34	6,81%
87	1,252	1,314	1,164	1,154	1,335	6,82%
97	1,246	1,31	1,157	1,148	1,328	6,84%
107	1,24	1,3	1,152	1,143	1,323	6,75%
117	1,235	1,295	1,145	1,136	1,316	6,79%
127	1,23	1,28	1,14	1,13	1,31	6,63%

Several simulations were done in all technology corners with the same result. This fact proves that the oscillation is highly dependent on all the parts of the signal path, providing an excellent fault coverage rate of 100% in open and short circuits for all corners.

3) *Parametric fault injection campaign*

This campaign was conducted by means of simulations using the five technology corners described above. Figure 7 shows oscillation frequency for all technology corners. In this case, the transistors channel width (W) was taken as a parameter.

As it can be seen, the circuit keeps oscillating in almost all corners within the range of +/- 5% (grey dotted lines) of the non-faulty frequency. This is good from the point of view of the robustness of the circuit facing changes in the technology, but is not useful in order to detect parametric changes between processes.

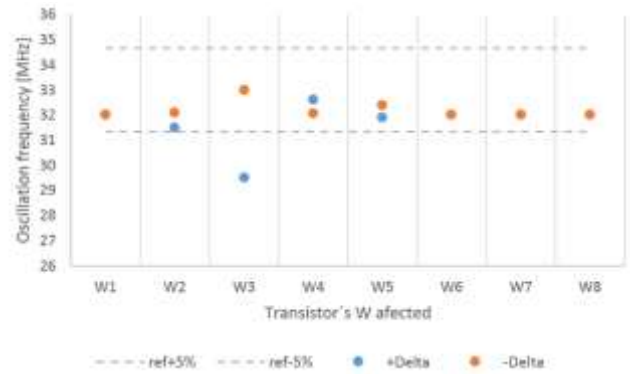


Fig. 7. Oscillation output as a function of different W's variations.

B. *OBIST Implementation*

The implementation of an OBIST scheme must be conducted analyzing the particular characteristics of the CUT and the tradeoff between test performance and hardware overhead. For our study case, the OBIST circuitry will be basically composed by a frequency-to-value converter (FVC) which converts the oscillation frequency to an N-bit value, and a control logic (CL) which executes all operations and produces the pass or fail test result [17]. This scheme is shown in Fig. 8.

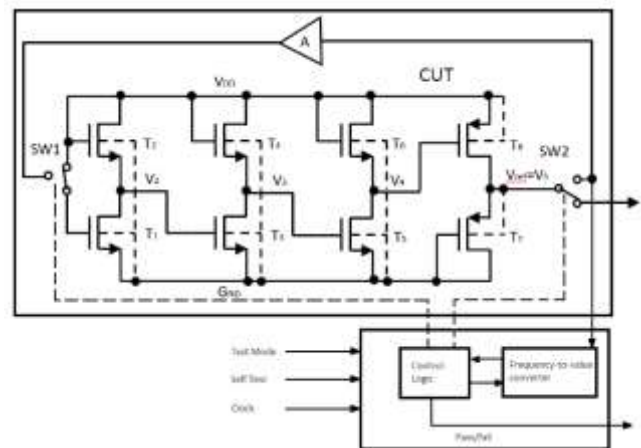


Fig. 8. Global view of the OBIST proposed structure.

When in test mode, switches SW1 and SW2 set the CUT in oscillation and the oscillation frequency is converted to a number (FVC) which is compared to a reference by CL. If the CL detects failure in oscillation (in our case there will be a lack of oscillation) it informs the failure condition. This process can be repeated as many times as needed.

If there is oscillation, a special circuit should be implemented in order to measure and compare the output frequency to a reference. The first step to accomplish this task should be to conform the oscillating signal level in order to make it compatible with the rest of the logic. One alternative to do this is using a Schmitt Trigger configuration such as shown in Fig. 9a.

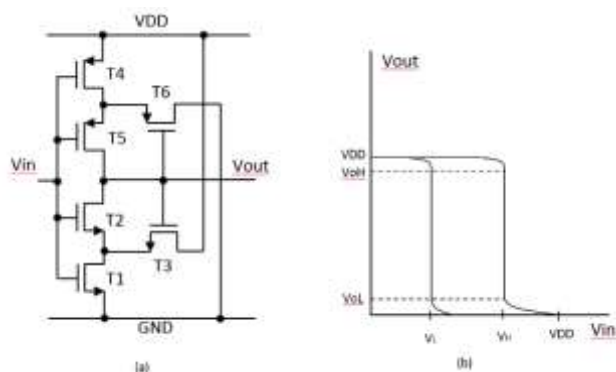


Fig. 9. a) Schmitt trigger schematic; b) transfer characteristic according to [18].

The threshold voltages of this circuit can be established in the proper way to conform the input signal. Fig. 9b shows the transfer characteristic of the circuit in Fig. 9a. Authors in [18] describe in detail the design procedure in order to set the threshold voltages for controlling the hysteresis. A possible set of values are shown in Table III.

TABLE III. TABLE III. COMPONENT SIZING FOR THE CIRCUIT OF FIG. 10.

Transistor	W/L [$\mu\text{m}/\mu\text{m}$]
T1	6/6
T2	18/6
T3	44/6
T4	14/6
T5	29/6
T6	70/6

The second stage to take into account is the frequency-to-value converter. This cell consists of a counter whose clock is controlled by a window-time generator, as is illustrated in Fig 10.

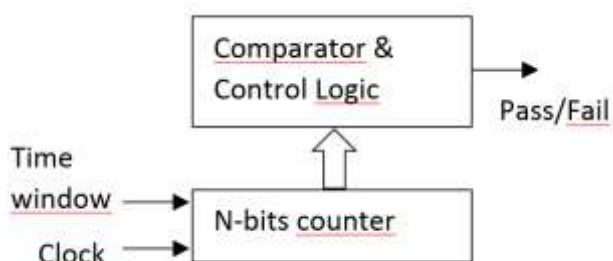


Fig. 10. Global scheme of the frequency-to-value block.

Finally, the CL block consists of a simple finite state machine which manages the whole system. At first, self-testing is performed in order to check functionality of the structure. After this, the Control Logic performs the rest of necessary tasks for completing the cell testing.

It should be noted that, in all simulated cases for every technology corner, the circuit produces no oscillation when catastrophic faults are injected. In this particular case, the FVC block could be avoided with the consequent simplification of the whole system. In this way, the detection and “pass/fail” parts of the system can be simply a capacitor and a diode as shown in Fig. 11.

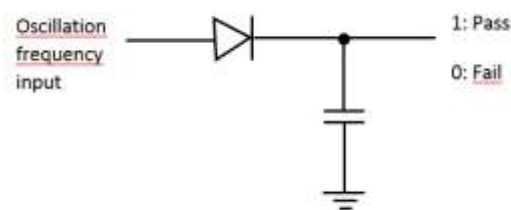


Fig. 11. Simplified pass/fail circuit.

If we consider the usage of this sensor cell embedded in the context of a system on chip (SoC) with a processor core, the so-called software-based BIST (SW-BIST) scheme could be implemented. In SW-BIST, an on-chip processor core functions as pattern generator and as response analyzer to test other components embedded in the system [19]. Under the assumption the above-mentioned elements are fault free, the approach of [20] can be applied in this case, where the processor core executes an embedded test routine that sequentially programs different CUT configurations (the OBT configuration in our case), acquires data from others peripherals, and performs required calculations to evaluate de CUT response. In this case, the only required peripheral is a simple timer with a compare-capture module. In capture mode, this module can measure the frequency of the CUT output signal configured as an oscillator. To apply the test procedure, an extra register for sensor reconfiguration is required. This proposal performs all verifications by using only the hardware and software resources of the SoC, minimizing consequently the cost in hardware overhead and power consumption.

As a last comment about signal path when converting the circuit into an oscillator, the adequate selection of the switches present in the OBT scheme (see Fig. 1 and 4) is very important because they provide the programmability of the structure, allowing the test. However, it is important to point out that these switches may affect the performance of the whole system in normal mode.

The main characteristics of these switches are their “on” and “off” resistances, named here RON and ROFF respectively. The values of these parameters must be carefully selected, depending on the place they are inserted [8, 18]. In this scheme, SW1 and SW4 are in the signal path, which means that they have to present very low RON in order to minimize their impact in the normal signal flow. On the other hand, SW2 and SW3 must have very high ROFF in order to adequately isolate the comparator from the CUT. Fig. 12 shows a typical scheme for implementing switches, the so-called pass-transistors.

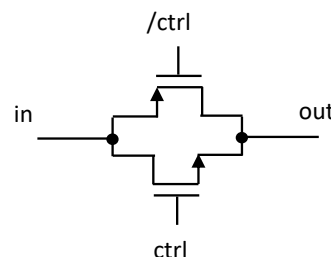


Fig. 12. Simple scheme for implementing the SW switches. Typical W/L values in used technology are 7.5 $\mu\text{m}/2\mu\text{m}$ for P transistor and 3 $\mu\text{m}/2\mu\text{m}$ for N transistor.

IV. CONCLUSION

An OBIST approach has been proposed for a fully analog dosimeter, the first to our best knowledge, and this scheme was applied in a system intended to be used for embedded applications. A test strategy for complete and accurate functional testing of the main cell has been developed using the proposed OBIST technique. In order to evaluate the approach, a catastrophic fault model was adopted at both device and circuit level. Despite the fact that circuit configuration robustness prevents the possibility of adequate detection of parametric faults, the catastrophic fault simulation shows a fault coverage of 100% for open and short circuits injected. The obtained results show extremely good data consistency and prove OBT becomes a very effective and reliable method for testing catastrophic faults in this case.

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